CLAIMS

1. A method of forming a self-aligned poly-metal stack over a semiconductor substrate by:

forming a multi-layer poly-metal structure over said semiconductor substrate;

forming an etch stop layer in a polysilicon region of said poly-metal structure;

removing portions of said poly-metal structure extending from an upper surface of said poly-metal structure to said etch stop layer to form a partial poly-metal stack including an exposed metal region and an upper polysilicon region along a sidewall of said stack;

covering said exposed metal region and said upper polysilicon region with an oxidation barrier layer; and

forming a full poly-metal stack including a lower polysilicon region aligned with said metal region and said upper polysilicon region along a sidewall of said stack.

2. A method as claimed in claim 1 wherein said full poly-metal stack is formed by removing at least a portion of said etch stop layer and a portion of said polysilicon region underlying said etch stop layer.

3. A method as claimed in claim 1 wherein said oxidation barrier layer is formed along at least a portion of said sidewall of said stack.

4. A method as claimed in claim 1 wherein said oxidation barrier layer is configured to cover said exposed metal region and said upper polysilicon region of said partial poly-metal stack without substantially covering said etch stop layer.

5. A method as claimed in claim 1 wherein said oxidation barrier layer is configured to cover said exposed metal region and said upper polysilicon region of said partial poly-metal stack so as to permit said removal of said etch stop layer and said polysilicon region underlying said etch stop layer.

6. A method as claimed in claim 1 wherein said oxidation barrier layer is configured to cover said exposed metal region and said upper polysilicon region of said partial poly-metal stack without substantially inhibiting removal of said etch stop layer and said polysilicon region underlying said etch stop layer.

7. A method as claimed in claim 1 wherein said full poly-metal stack further comprises an exposed oxide region aligned with said exposed metal region, said upper polysilicon region, and said lower polysilicon region.

8. A method as claimed in claim 7 wherein said process further comprises interfacing said poly-metal stack and said semiconductor substrate by subjecting said exposed oxide region to an oxidation process.

9. A method as claimed in claim 8 wherein said poly-metal stack and said semiconductor substrate are interfaced through selective oxidation.

10. A method as claimed in claim 8 wherein said poly-metal stack and said semiconductor substrate are interfaced through non-selective oxidation.

11. A method as claimed in claim 8 wherein said poly-metal stack and said semiconductor substrate are interfaced through oxidation by H_2 and H_20 derived from catalytic conversion of H_2 and O_2.

12. A method as claimed in claim 8 wherein:

said poly-metal stack and said semiconductor substrate are interfaced through oxidation by H_2 and activated O_2; and

said activated O_2 is derived through activation by a remote plasma unit.

13. A method as claimed in claim 1 wherein said etch stop layer is formed within said polysilicon region.

14. A method as claimed in claim 1 wherein said etch stop layer is formed in said polysilicon region through ion implantation.

15. A method as claimed in claim 1 wherein:

said poly-metal structure is formed through a plurality of structural layering steps; and

said etch stop layer is formed in said polysilicon region through an intermediate layering step of said plurality of layering steps.

16. A method as claimed in claim 1 wherein said poly-metal structure is formed such that said metal layer comprises tungsten.

17. A semiconductor structure comprising:

a semiconductor substrate;

a multi-layer self-aligned poly-metal stack formed over said semiconductor substrate, wherein said poly-metal stack comprises a metal region, an upper polysilicon region, and a lower polysilicon region aligned along a sidewall of said stack;

an oxidation barrier layer formed along a portion of said sidewall of said poly-metal stack covering said metal region and said upper polysilicon region; and

an oxidized layer formed along a portion of said sidewall of said poly-metal stack covering said lower polysilicon region, wherein said oxidized layer and said oxidation barrier layer interface along said sidewall at a boundary defined between said upper and lower polysilicon regions.

18. A semiconductor structure as claimed in claim 17 wherein said poly-metal stack further comprises an insulating layer formed over said metal layer.

19. A semiconductor structure as claimed in claim 18 wherein said insulating layer is aligned with said metal region, said upper polysilicon region, and said lower polysilicon region along said sidewall of said stack.

20. A semiconductor structure as claimed in claim 18 wherein said insulating layer comprises a silicon dioxide layer.

21. A semiconductor structure as claimed in claim 18 wherein said oxidation barrier layer formed along a portion of said sidewall of said poly-metal stack covers said insulating layer.

22. A semiconductor structure as claimed in claim 17 wherein said oxidized layer further covers an oxide region of said poly-metal stack along said sidewall of said stack.

23. A semiconductor structure as claimed in claim 17 further comprising an etch stop layer formed in said poly-metal stack.

24. A semiconductor structure as claimed in claim 23 wherein said oxidized layer and said oxidation barrier layer interface along said sidewall at a point defined by said etch stop layer.

25. A semiconductor structure as claimed in claim 23 wherein said etch stop layer is formed between said upper and said lower polysilicon regions of said poly-metal stack.

26. A semiconductor structure as claimed in claim 23 wherein said etch stop layer comprises a conductive etch stop layer.

27. A memory cell array comprising an array of wordlines and digitlines arranged to access respective memory cells within said array, wherein respective ones of said wordlines comprise a multi-layer self-aligned poly-metal stack formed over said semiconductor substrate, wherein:

said poly-metal stack comprises a metal region, an upper polysilicon region, and a lower polysilicon region aligned along a sidewall of said stack;

an oxidation barrier layer is formed along a portion of said sidewall of said poly-metal stack covering said metal region and said upper polysilicon region; and

an oxidized layer is formed along a portion of said sidewall of said poly-metal stack covering said lower polysilicon region, wherein said oxidized layer and said oxidation barrier layer interface along said sidewall at a boundary defined between said upper and lower polysilicon regions.

28. A computer system comprising a memory cell array in communication with a microprocessor via a data communication path, wherein:

said memory cell array comprises an array of wordlines and digitlines arranged to access respective memory cells within said array;

respective ones of said wordlines comprise a multi-layer self-aligned poly-metal stack formed over said semiconductor substrate;

said poly-metal stack comprises a metal region, an upper polysilicon region, and a lower polysilicon region aligned along a sidewall of said stack;

an oxidation barrier layer is formed along a portion of said sidewall of said poly-metal stack covering said metal region and said upper polysilicon region; and

an oxidized layer is formed along a portion of said sidewall of said poly-metal stack covering said lower polysilicon region, wherein said oxidized layer and said oxidation barrier layer interface along said sidewall at a boundary defined between said upper and lower polysilicon regions.